CONFIDENTIAL B

MMD (MediaTekModuleDesign) Plan

MT6799 MMD User Guide

V0.4

History

Version	Date	Description	Description
V0_1	2016/6/3	First release.	Chunhua, Jianghong ,Matt, FK Pan
V0_2	2016/7/5	1.VPROC separate to VPROC1&VPROC2; 2.Update DVDD_SRAM_GPU 3.Update RFIC_ET0_P/N 4.Update DVDD_IOETC Power	Chunhua, Jianghong ,Matt, FK Pan
V0_3	2016/8/10	1.Update 10LHDI-2 plus GND 2.Add 10LHDI3 and ELIC	Chunhua, Jianghong ,Matt, FK Pan
V0_4	2016/12/14	1.In line with the Reference design V0.5 2.Update the L2101 L2102 L2103 decal 3.Merge the VA10_PMU,VA12_PMU,and update the fan-out 4.Delete the co-lay parts 5.Update the PDN caps' Name and optimize the PDN solution	Chunhua, Jianghong ,Matt, FK Pan

Foreword

Since smart phone design is going to be lighter, thinner and with larger battery capacity, its PCB design will be more complicated in order to satisfy good performance of the Power Delivery Network (PDN), high-frequency CPU and mobile memory.

In order to help customer to design "<u>Correct</u>", "<u>Excellent</u>" and "<u>Reliable</u>" smart phone PCB, this slide introduce **MediaTek Module Design (MMD),** and provide methods to implement module designs of PDN & eMCP. The purposes of MMD are helping customer to reduce time of PCB design, ensure system perforr a e possible and significantly reduce test and debug efforts. Final target is help customer promote products to market as soon as possible.

Outline

- Introduction of schematic and PCB layout module
- PCB layout module description and user guide
- Implement method of PCB layout module

Introduction of Schematic and PCB Module

What is schematic and PCB module?

- Make the “verified” schematic and PCB layout to be a particular layout design, which could be reused on similar products in the future.

Application of schematic & PCB module

- Please use MTK’s schematic to design your circuit and keep the net name is same with MMD when you imported MMD design.
- Please import the module when placement is done and before you do PCB layout.

Notice of implement PCB layout module

- Main power capacitors’ placement, routing and via (include GND via)
  (Main power: VDD2, VDDQ,VMODEM_PMU, VCORE_PMU,VMD1_PMU,VIMVO_PMU, DVDD_PROC1, DVDD_PROC2, DVDD_GPU, VSRAM_GPU_PMU, VSRAM_MD_PMU, VSRAM_CORE_PMU, VSRAM_DVFS1_PMU, VSRAM_DVFS2_PMU,VA10_PMU,VA12_PMU)
- MT6799 whole chip fan-out
- MT6335 input caps’ placement and layout design notice

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- Introduction of schematic and PCB layout module
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Module Format and Type

- **EDA tool format**
  - SCH: Orcad and PADs logic
  - PCB file:
    - Layout file PADs9.3.1
    - Asc file PADs2005.2

- **Module type**
  - EMI
    - Discrete_LPDDR4X_POP_376b
  - PCB Structure
    - 10L HDI3 (stack via)
    - ELIC
  - BB capacitors placement
    - Double- Side

PCB layout module list

- MT6799 PCB layout module list

Module	PCB Layer& Stack-up	Component placement	Via type	PCB Number	Module name
Discrete_LPDDR 4X_POP_376b	10L HDI-3 (stack via)	Double-side	3+4+3 (Stacked via)	MTK0069-4	MT6799_MMD_Discrete_LPDDR4X_POP_376b_10L HDI3_Double-side_V0_4
Discrete_LPDDR 4X_POP_376b	10L ELIC (stack via)	Double-side	Anylayer	MTK0069-6	MT6799_MMD_Discrete_LPDDR4X_POP_376b_10L ELIC_Double-side_V0_4

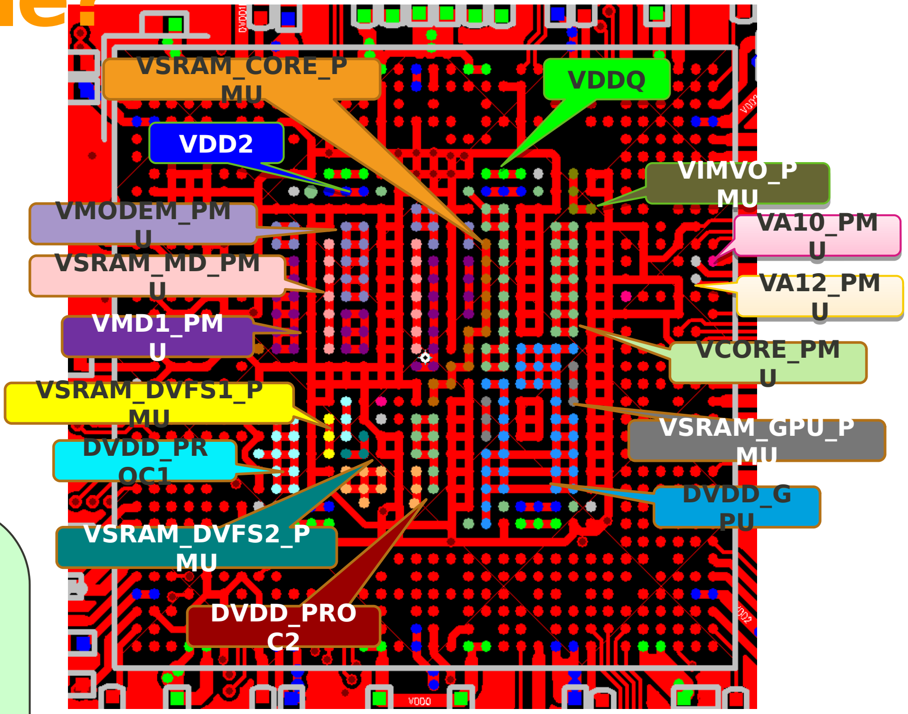
How to choose and use the suitable PCB module?

Decide your PCB stackup, Layers

Find the corresponding PCB number from “MT6799 PCB Layout Module list”, and get the right SCH & PCB

Completely implement **VDD2, VDDQ,VMODEM_PMU, VCORE_PMU,VMD1_PMU,VIMVO_PMU, DVDD_PROC1, DVDD_PROC2, DVDD_GPU, VSRAM_GPU_PMU , VSRAM_MD_PMU, VSRAM_CORE_PMU, VSRAM_DVFS1_PMU, VSRAM_DVFS2_PMU , VA10_PMU,VA12_PM traces, vias (include GND), copper (including GND plane)** to your PCB design and finish other region.

※ Note: If the module design need to be adjusted, please follow the latest PCB design guideline.



Note：If any question, please feel free to contact correlative engineers of MediaTek.

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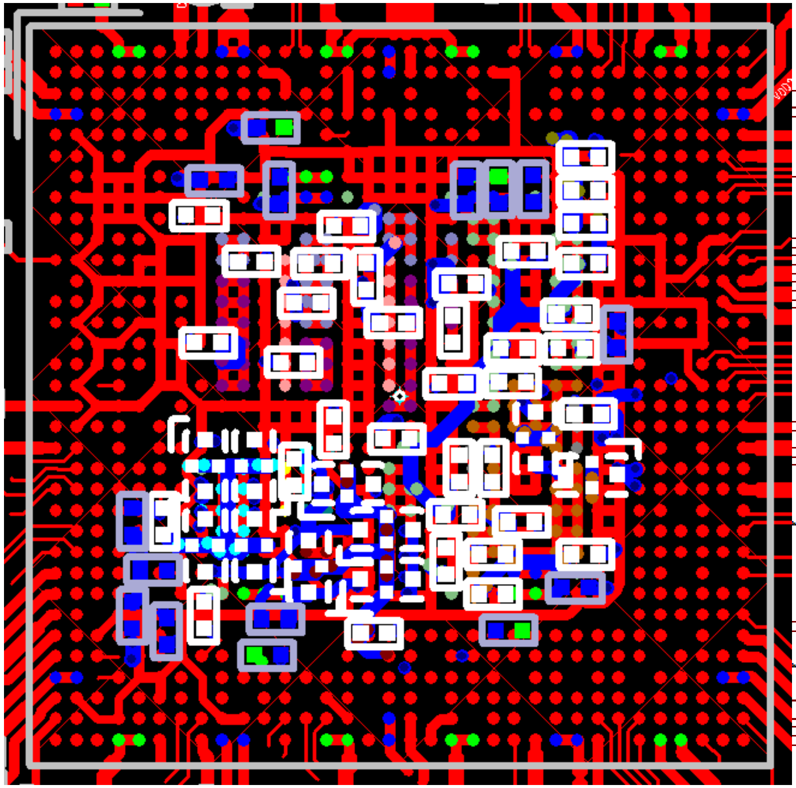
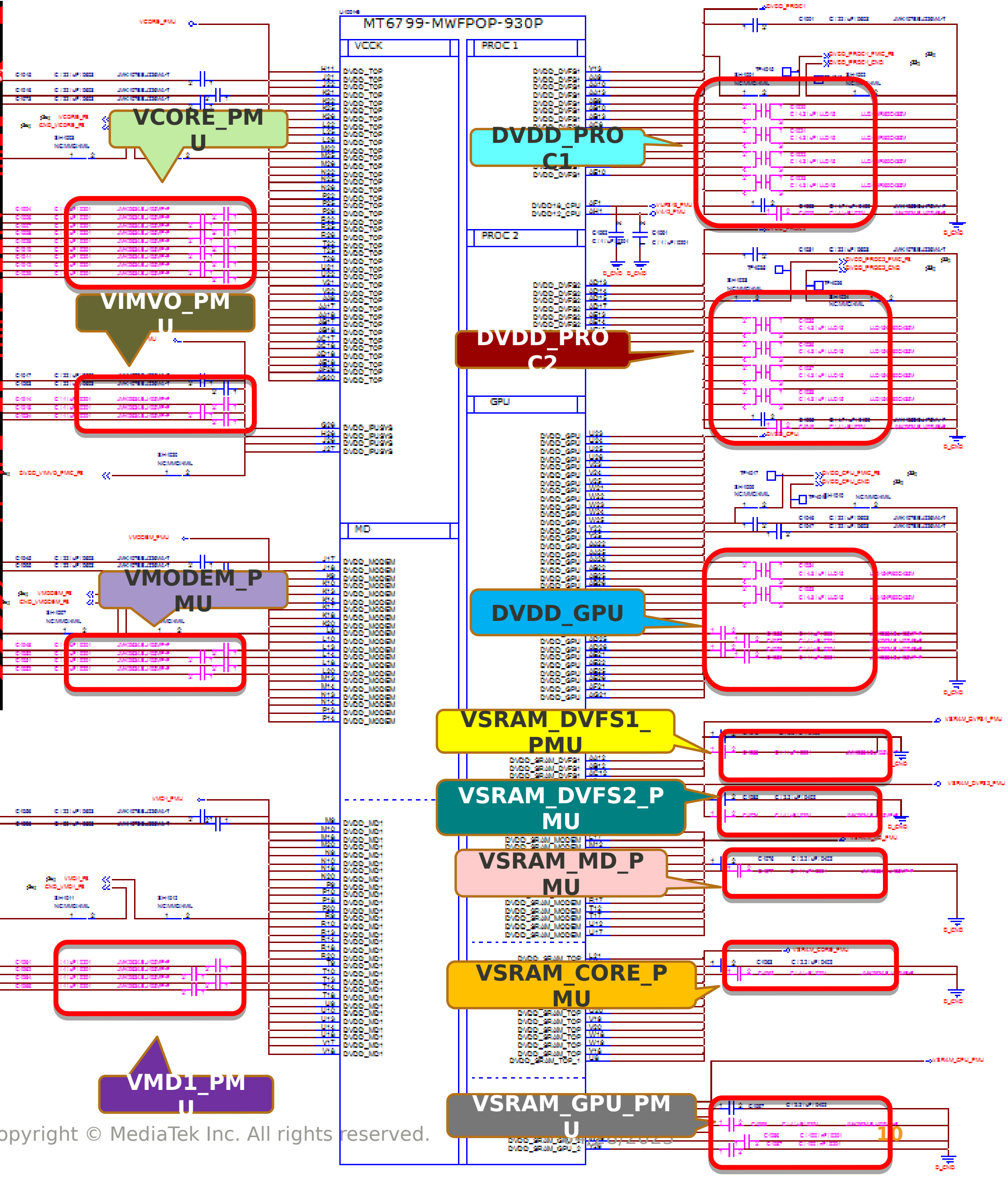
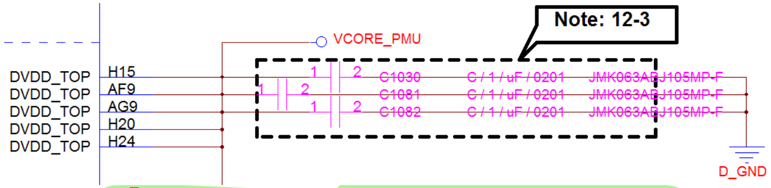
Key Components groups to PDN Design (1/4)







※ **Note:**
The highlight capacitors must be closed to MT6799.

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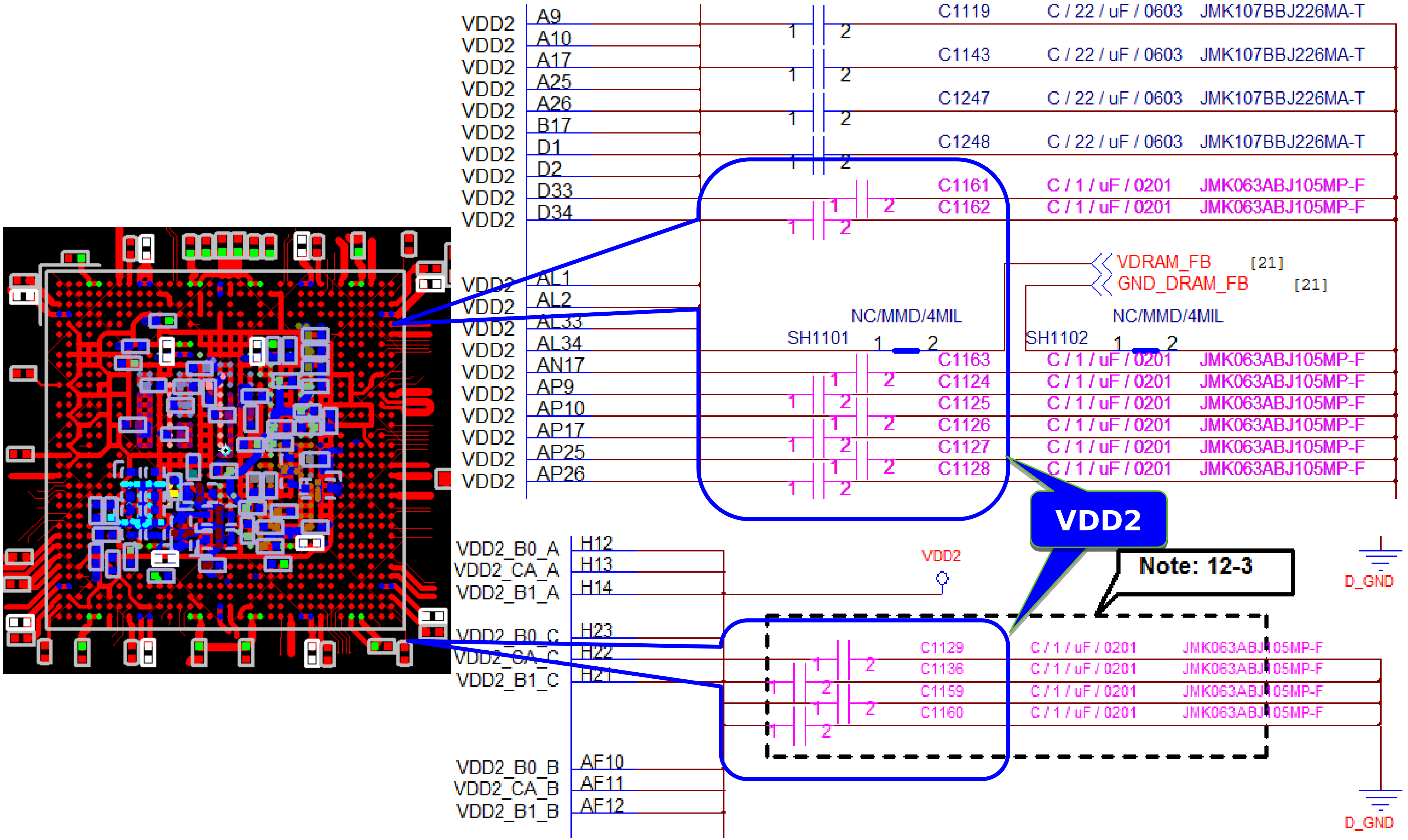
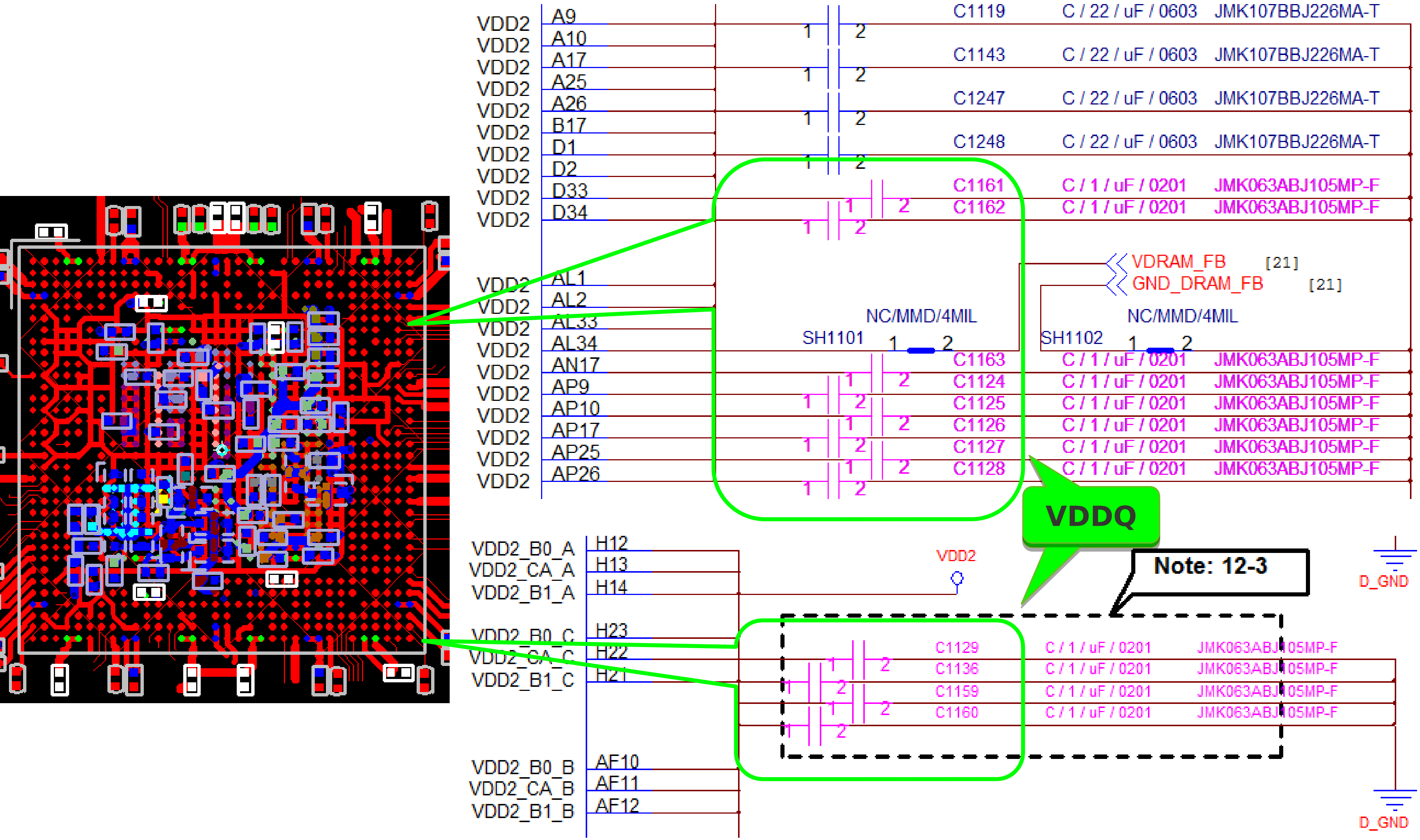
Key Components groups to PDN Design (2/4)



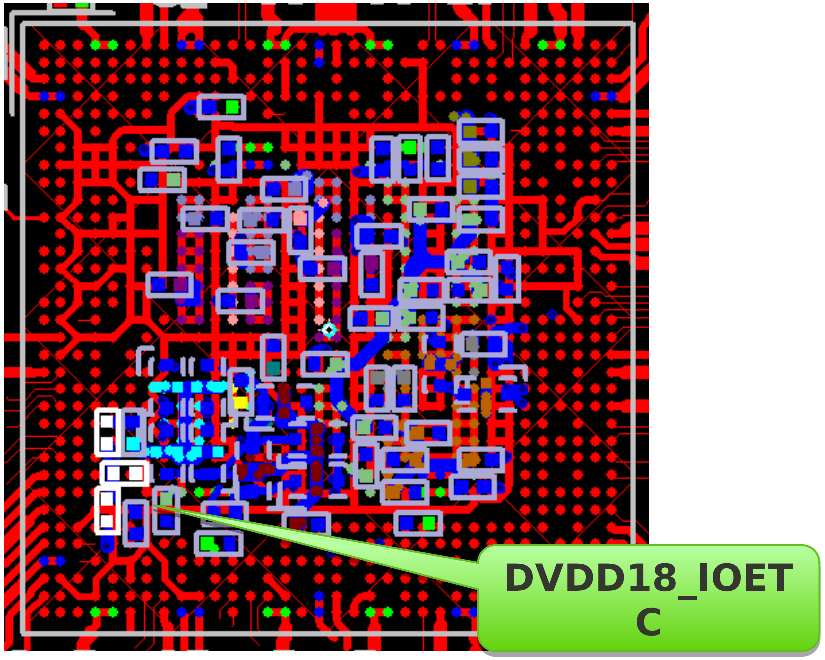
※ **Note:** The highlight capacitors must be closed to MT6799.

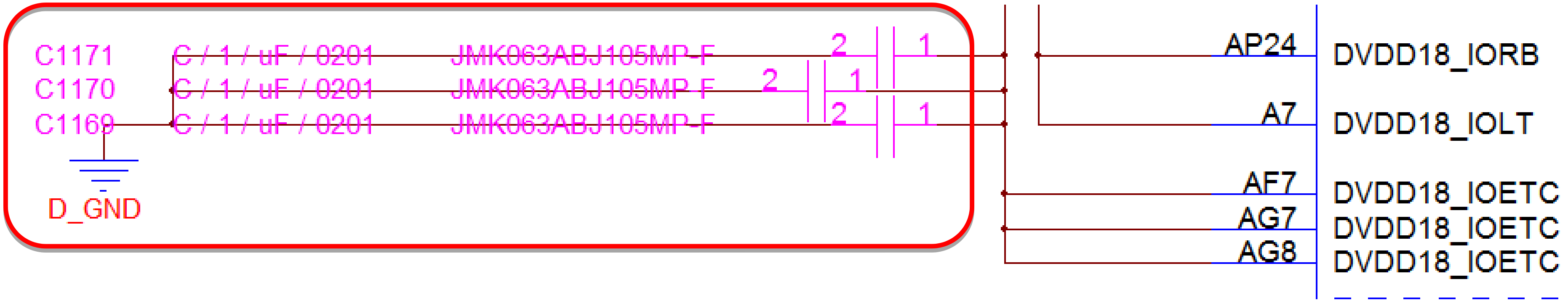
Key Components groups to PDN Design (3/4)



※ **Note:** The highlight capacitors must be closed to MT6799.

■ Key Components groups to PDN Design (4/4)





※ **Note:** The highlight capacitors must be closed to MT6799.

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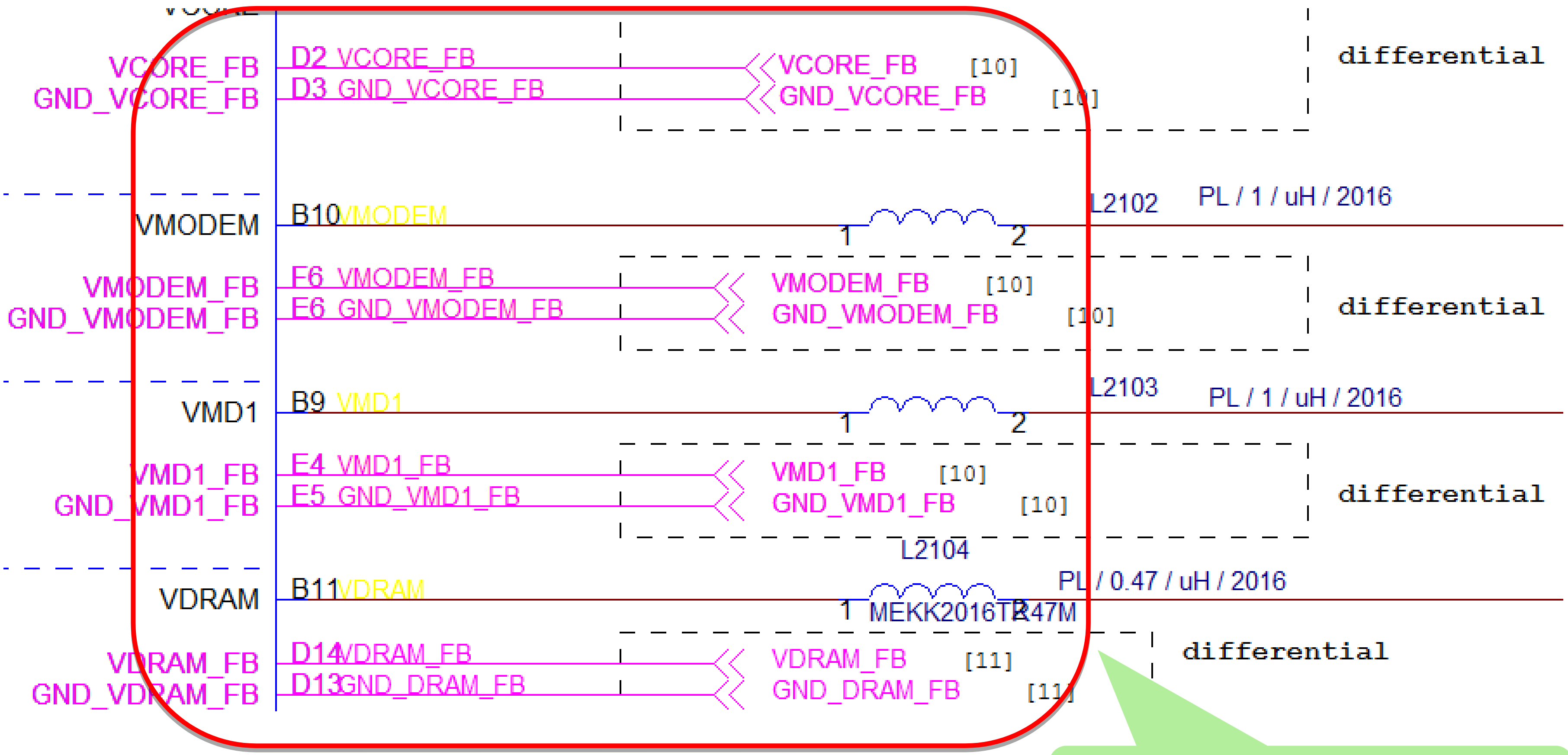
■ FB signals to PDN Design (1/3)



Routed at differential pairs

※ Note:
Those signals are differential pairs and should be shielded by GND and far away from noise signals

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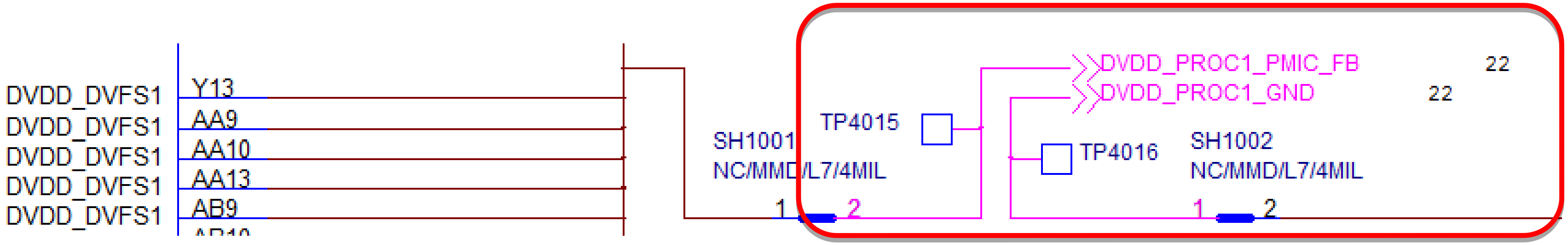
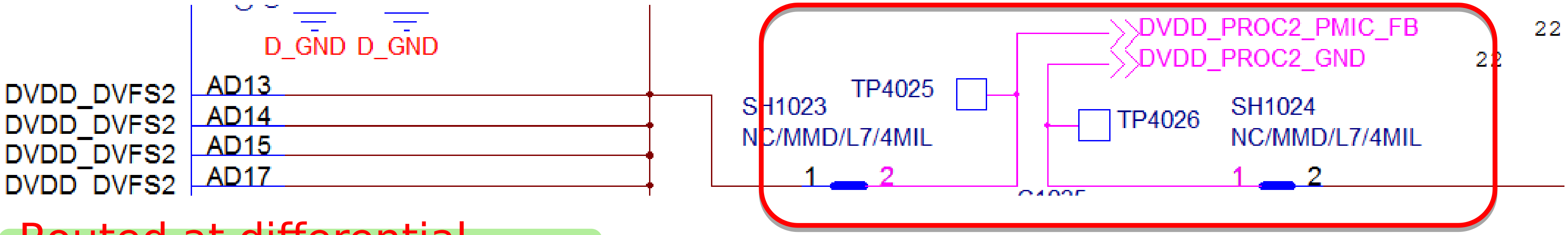
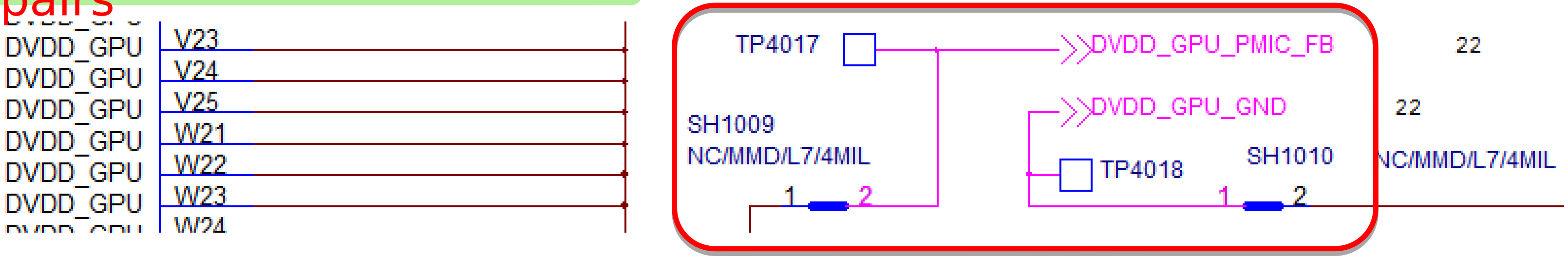
■ FB signals to PDN Design (2/3)





Routed at differential pairs



※ Note:

Those signals are differential pairs and should be shielded by GND and far away from noise signals

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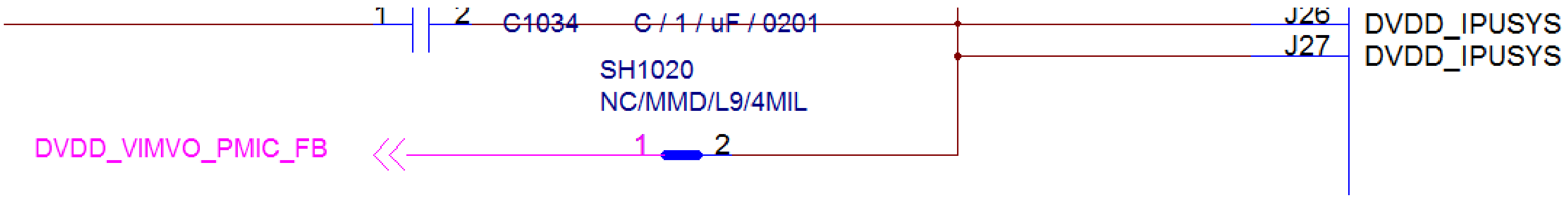
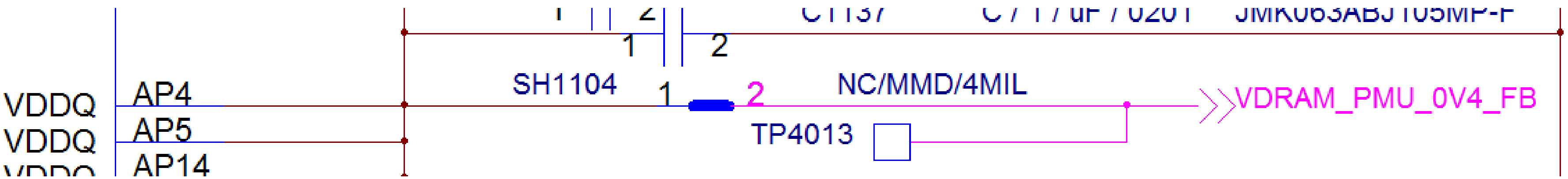
■ FB signals to PDN Design (3/3)





※ **Note:**
Those signals should be shielded by GND and far away from noise signals

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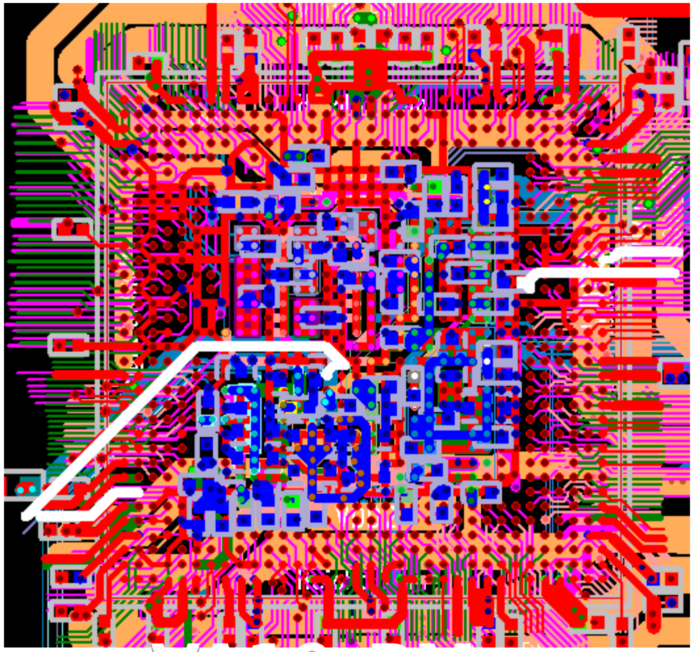
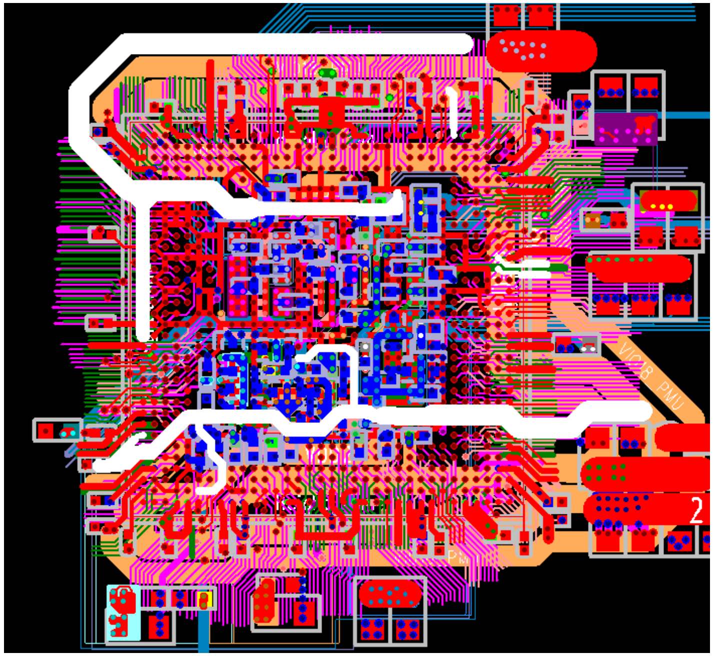
■ VA10_PMU &VA12_PMU IR Drop



VA10_PMU

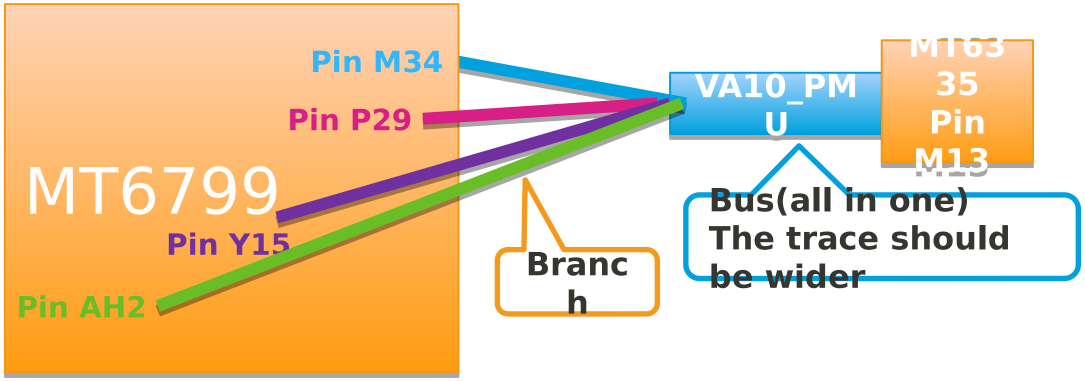


VA12_PMU

※ Note:

1 AVDD09 ,AVDD12 had better separate from MT6335 part and route as star-lines

Take VA10_PMU for example:



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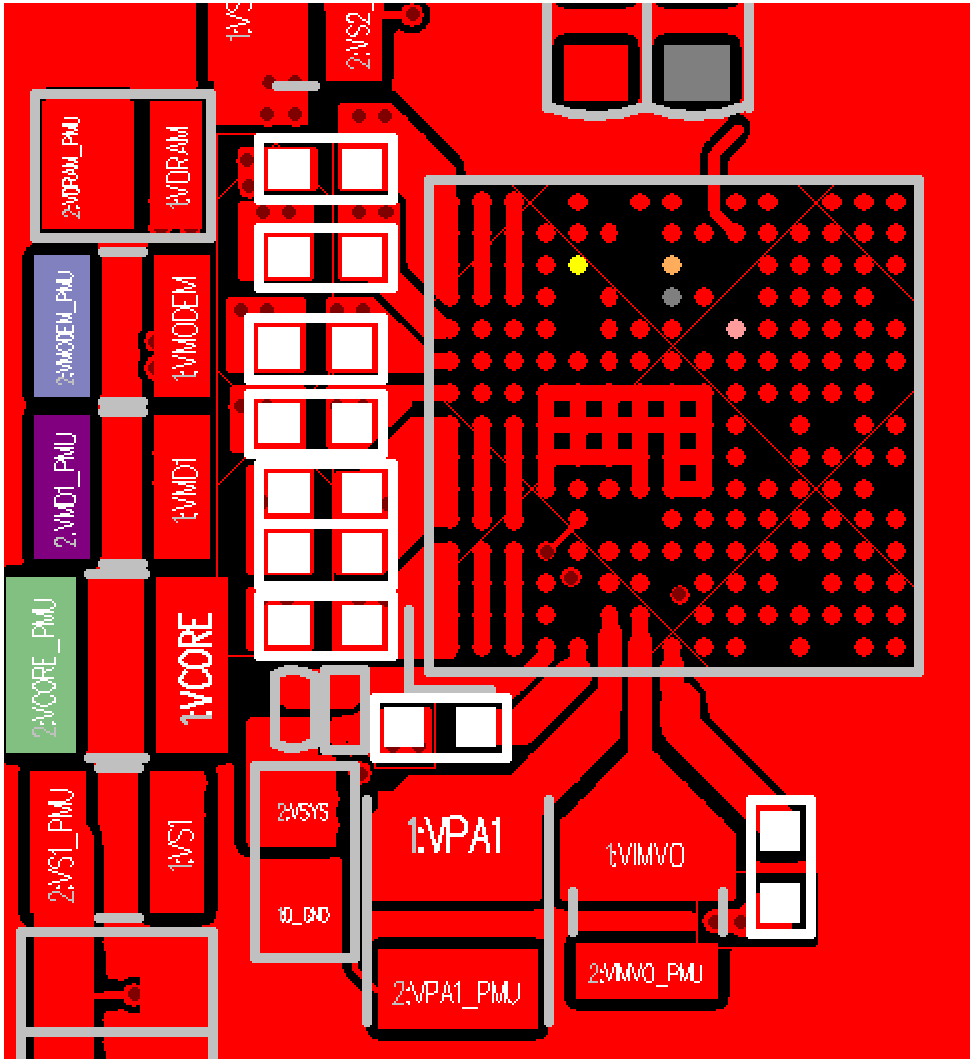
■ Key Components to PMIC Design for MT6335 (1/3)



※ **Notice:**

Must follow the Cap placement and routing in MMD fully.

All the highlight decoupling capacitors should be placed near to MT6335.The priority is buck capacitor and then decoupling capacitor of LDO.

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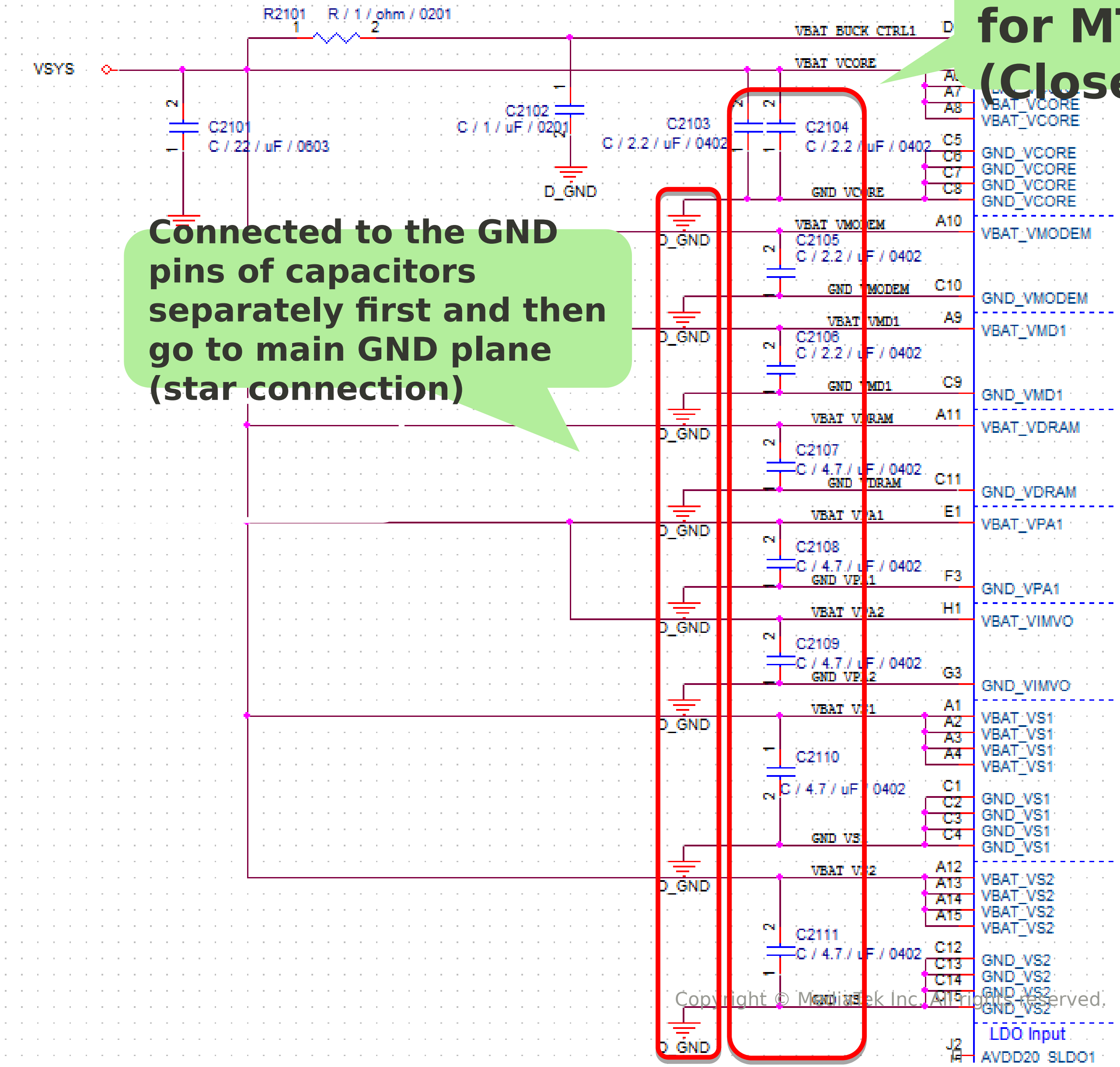
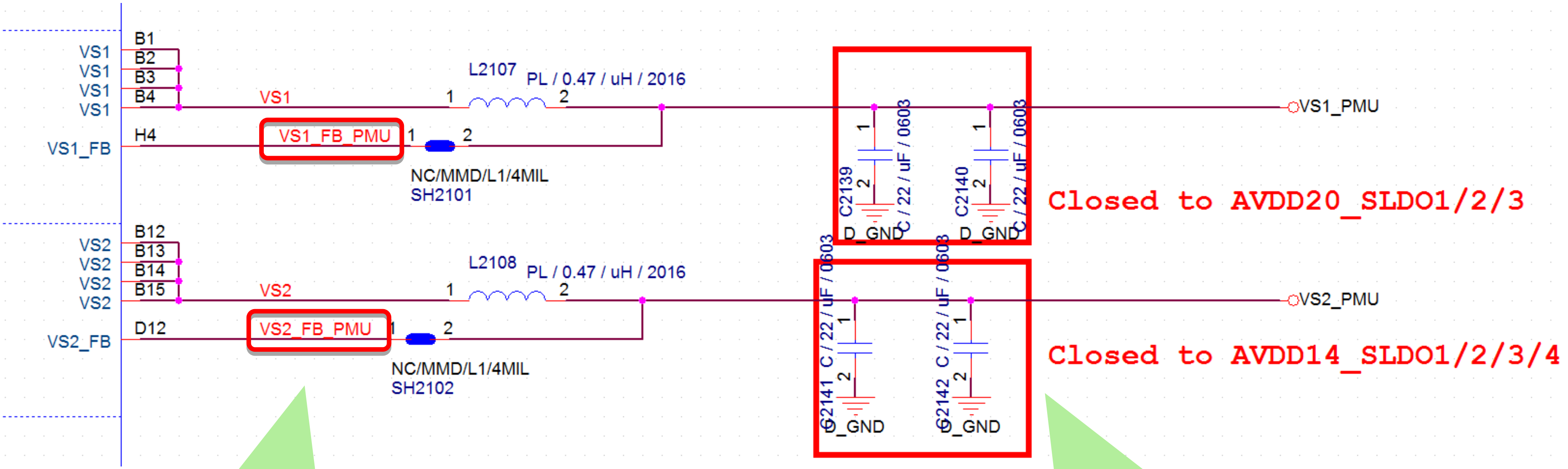
Key Components to PMIC Design for MT6335(2/3)

Key Components for MT6335 (Close to PMIC)

Connected to the GND pins of capacitors separately first and then go to main GND plane (star connection)



Key Components to PMIC Design for MT6335(3/3)



The feed-back signals should directly come from the output caps and have good ground shielding.

Key Components for MT6335 (Close to PMIC LDO input balls)

Highlight (PMIC critical input cap placement)

MT6335 Design Notice
Rule1: Buck ctrl signal (VBAT_Buck_CTRL) pin(ball D1) connect to output bypass capacitor(C2102) directly.
Rule2: Buck GND balls are separately connected to buck capacitors(C2104~C2111) with planes or trace(≧20mil) then connected to main GND .
Rule3: VBAT/GND/VBAT_BUCK_CTRL trace length requirement: C2104~C2111 Capacitors must close to MT6335 (The best is the same as MMD design) VBAT_BUCK_CTRL ball to Capacitor ≤120mil
Rule4: VS1_FB(Ball H4) need to be connected to capacitors (C2139/C2140).
Rule5: VS2_FB(Ball D12))need to be connected to capacitors (C2141/C2142).

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Outline

- Introduction of schematic and PCB layout module
- PCB layout module description and user guide
- Implement method of PCB layout module

- **Implement method in different situations**
  - Fully implement MMD
  - Different footprint
  - Different placement design
  - Different net name
- **Application of different EDA tool translation**

Fully Implement MMD

- **Schematic requirement**
  - Make sure your correlative schematic of module is same with MMD.
- **Placement requirement**
  - BB’s placement should be same with MMD.
- **How to implement MMD**
  - Method 1:
    - Import new netlist to module PCB directly.
  - Method 2:
    - Copy module design into existent PCB by reuse function.

Different Footprint

- **Schematic requirement**
  - Keep correlative schematic of module part is same with MMD except footprint name. (Reference & Net name should be same with MMD)
- **How to implement MMD**
  - Method 1
    - Step 1: Change MMD footprints according to customer's footprint libraries by "Find → Part Type".
    - Step 2: Copy module design into the existing PCB by reuse function.
  - Method 2
    - Step 1: Get the components' coordinate by exporting emp/emn files and import them to your design.
    - Step 2: Copy traces, vias, and copper in the module to the existing PCB by reuse function.

Note: If fine-tuning of the module layout is unavoidable, Please follow the latest "PCB Design Guideline".

Different Placement Design

- **Schematic requirement**
  - Make sure correlative schematic of module part is same with MMD.
- **How to implement MMD**
  - Step1 : Individually copy MT6799 & MT6335 trace, via, and copper into your PCB design.
  - Step2 : Finish the remaining connections according to the design guideline.

In order to individually adjust each module’s location , partial copy module design and more effectively use the narrow space, separately reuse is recommended.

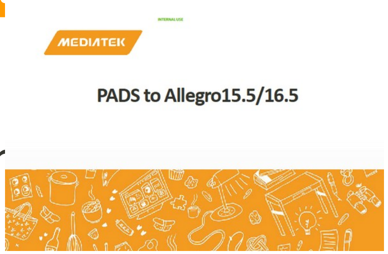
PDN is the most critical design in smart phone. Ensure design performance and efficiency, we strongly recommend you take the advantages of MMD module as much as you can.

Different Net Name

- **Schematic requirement**
  - Modify the correlative schematic to keep the same with MMD when the net name is different.
- **How to implement MMD**
  - Method 1
    - Step 1: Modify “net name” to be the same with MMD.
    - Step 2: Copy MMD module according to the method of fully implement MMD.
  - Method 2
    - Step 1: Copy MMD module into your design on ECO mode.
    - Step 2: Select traces, vias, and copper in the added module, and copy them to the right place in one design.
    - If a few modifications are unavoidable, follow the latest “PCB Design Guideline”.

Translation Skill Between Different EDA Tools

- Cadence Allegro
  - Refer to the attachmen



- Mentor Expedition
  - Refer to the attachment “Pads to Expec

- Other EDA tools
  - Contact your EDA tool vendor.

MediaTek Contact Windows

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